REMARKS

A Petition and Fee for Three Month Extension of Time is submitted herewith.

Claims 1-20 are all the claims presently pending in the application. Claims 1-2 have been amended and claims 3-20 have been added to claim additional features of the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1 and 2 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Han et al. (U.S. Patent No. 5,926,235) in view of Park et al. (U.S. Patent No. 6,380,559) further in view of Baek (U.S. Patent No. 6,256,077) further in view of Rho et al. (U.S. Patent No. 6,243,146).

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as defined by claim 1) is directed to a liquid crystal display device which includes a plurality of pixels arranged in a matrix form, each of the pixels includes a pixel electrode formation area wherein a pixel electrode is formed, and a thin film transistor formation area wherein a thin film transistor is formed and connected to the pixel electrode.

Further, the thin film transistor includes a semiconductor layer serving as a channel, a terminal formed to be connected to the pixel electrode, a passivation layer formed to cover the thin film transistor, and an organic insulating layer covering the passivation layer. The semiconductor layer extends from the channel toward the pixel electrode formation area beyond the terminal and terminated in the pixel electrode formation area to form a termination end that is aligned with a termination end of the passivation layer, and the organic insulating layer covers the termination ends of the semiconductor layer and the passivation layer. Importantly, the pixel electrode formation area includes a plurality of prism-shaped base posts, and an uneven layer formed on the plurality of prism-shaped base posts.

Conventional liquid crystal displays have attempted to improve performance by forming uneven using an organic insulating layer on an active matrix substrate and forming a reflection electrode thereon (Application at page 6, lines 1-5). However, such attempts complicate the manufacturing steps and decrease productivity (Application at page 7, lines 15-20).

The claimed invention, on the other hand, includes a pixel electrode formation area having a plurality of prism-shaped base posts, and an uneven layer formed on the plurality of prism-shaped base posts (Application at page 26, line 5-page 27, line 27; Figures 13-14B). The base posts can be formed at the time of forming the gate insulating film, semiconductor layer, and passivation film in the transistor, and therefore, requires fewer manufacturing steps than conventional devices (Application at page 27, lines 16-24).

II. THE HAN, PARK, BAEK, AND RHO REFERENCES

The Examiner alleges that Han would have been combined with Park, that a Han/Park combination would have been further combined with Baek, and that the combination of Han/Park/Baek would have been further combined with Rho to form the claimed invention. Applicant submits, however, that these references would not have been combined, and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

First, Applicant points out that the Examiner has been required to combine no less than four references to reject the claimed invention. Applicant respectfully submits that this alone evidences the novelty of the claimed invention (as well as the Examiner's hindsight reconstruction), and makes clear the Examiner's failure to make a prima facie case of obviousness.

Han discloses an active matrix liquid crystal display (AMLCD). Han intends to provide a method for fabricating the device which has a minimal number of masking steps. The method includes forming a first passivation layer which covers storage capacitor, drain electrodes, semiconductor layer, source bus lines and source electrodes, and then forming a second passivation layer which covers the first passivation layer and the substrate (Han at Abstract).

Park discloses a thin film transistor substrate for a liquid crystal display that includes an insulating substrate, and a gate line assembly formed on the substrate. Park intends to provide a method for fabricating the device which has a minimal number of masking steps. In the Park substrate, a black matrix and a color filter may be formed at the structured substrate before forming the pixel electrode, and an opening portion may be formed between the pixel electrode and the data line (Park at Abstract).

Baek discloses a thin film transistor array for an LCD device which is allegedly formed in four photolithography steps. This is allegedly accomplished by patterning a passivation layer, gate insulating layer and semiconductor layer in a single step, and forming an etch protection layer on a gate line on both sides of a data line (Baek at col. 1, lines 45-50).

Rho discloses a liquid crystal display in which a passivation layer is formed by coating a flowable insulating material on the substrate where a thin film transistor and a storage capacitor electrode, and a pixel electrode is formed on the passivation layer. A portion of the passivation layer is etched using the pixel electrode as a mask to make a groove on the thin film transistor, and then a black matrix is formed by filling an organic black photoresist in the groove (Rho at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions. Indeed, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner merely states that it would have been obvious to combine these references "in order to have a liquid crystal display device with better performance". However, there is no reason to suggest why such a combination would result in better performance. Using the Examiner's reasoning any two (or four) references could be combined to "achieve better performance". Obviously, this is fallacious reasoning.

Applicant notes that the Examiner has failed to support the alleged combination with specific suggestions or motivation from any of the references. In fact, Applicant respectfully submits that there is no such motivation or suggestion to combine the references, and one of

ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, neither Han, nor Park, nor Baek, nor Rho, nor any combination thereof teaches or suggests "*wherein said pixel electrode formation area comprises a plurality of prism-shaped base posts, and an uneven layer formed on said plurality of prism-shaped base posts*", as recited, for example, in claim 1.

As noted above, unlike conventional liquid crystal displays, the claimed invention includes a pixel electrode formation area having a plurality of prism-shaped base posts, and an uneven layer formed on the plurality of prism-shaped base posts (Application at page 26, line 5-page 27, line 27; Figures 13-14B). The base posts can be formed at the time of forming the gate insulating film, semiconductor layer, and passivation film in the transistor, and therefore, requires fewer manufacturing steps than conventional devices (Application at page 27, lines 16-24).

Clearly, these features are not taught or suggested by any of the cited references. Indeed, Applicant points out that the Examiner does not even address this feature in the Office Action. The Examiner certainly does not attempt to identify any teaching or suggestion of these features in the cited references. In fact, nowhere are these features taught or suggested by the cited references.

For example, Han discloses a formation of thin film transistors on a substrate in an LCD device (e.g., Han at Figure 5I). Han teaches a conventional design in which a pixel electrode 104 is connected to a storage capacitor 130. However, nowhere does Han teach or suggest a plurality of base posts in a pixel electrode formation area, let alone a plurality of prism-shaped base posts, or an uneven layer formed on the plurality of prism-shaped base posts.

Similarly, Park does not teach or suggest the novel features of the claimed invention. Indeed, like Han, Park is merely directed to the formation of the thin film transistors is not concerned with a pixel electrode formation area. For example, Park merely discloses a pixel electrode 82 which are connected to thin film transistors 3 (Park at Figure 2; col. 7, lines 8-22). Thus, nowhere does Park teach or suggest a pixel electrode formation area having a

plurality of prism-shaped base posts, and an uneven layer formed on the plurality of prism-shaped base posts.

Baek, like Park, merely discloses a pixel electrode 84 connected to a thin film transistor (Baek at Figure 3; col. 3, lines 13-19). Clearly, Park does not teach or suggest a pixel electrode formation area having a plurality of prism-shaped base posts, and an uneven layer formed on the plurality of prism-shaped base posts.

Like the other references, Rho does not teach or suggest the novel features of the claimed invention. Indeed, Rho merely discloses a pixel electrode 140 which is connected to a thin film transistor (Rho at Figure 3; col. 5, lines 40-45). Nowhere does Rho teach or suggest a plurality of base posts formed in a pixel electrode formation area, let alone the other novel features of the claimed invention.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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